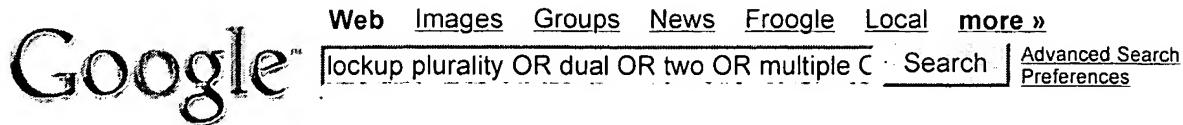


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Web Results 1 - 10 of about 587 for **lockup plurality OR dual OR two OR multiple OR parallel "scan path|chain|string..."**

Phone Conference P1450

Lockup: This is a pre-defined cell type that is used to identify "lockup latches" which are placed in the **scan chain** typically for the purpose of ...

grouper.ieee.org/groups/1450/dot1/minutes-2003-11-06.html - [Similar pages](#)

DS21Qx5y BSDL Scan Chain Mapping - Maxim/Dallas

JTRST, JTCLK, and JTMS are wired together in **parallel**. To complete the **scan chain**, four copies of the specific DS21x5y BSDL file need to be placed in the ...

www.maxim-ic.com/appnotes.cfm/appnote_number/406 - 78k - [Cached](#) - [Similar pages](#)

10 tips for successful scan design: part one - 2/17/2000 - EDN

Lockup latches are nothing more than transparent latches. You use them to connect **two** scan-storage elements in a **scan chain** in which excessive clock skew ...

www.edn.com/article/CA46603.html - [Similar pages](#)

10 tips for successful scan design: part two - 2/17/2000 - EDN

The first problem is within a design block that contains **multiple** drivers ...

Therefore, you should insert a **lockup** latch in the **scan chain** before and after ...

www.edn.com/article/CA46604.html - [Similar pages](#)

[[More results from www.edn.com](#)]

On-time Finish Rests With Multiple Clocks

This means that if **multiple** clocks are used within the same **scan chain**, ...

In this example, each **scan chain** has **two** scan cells, and there is a total of ...

www.us.design-reuse.com/articles/article2820.html - 56k - [Cached](#) - [Similar pages](#)

[PDF] Efficient Scan Chain Design for Power Minimization During Scan ...

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in **two** steps: the first one consists in determining the chaining of the scan cells so as to ... **multiple** clock domains and **lockup** latches. Also, work ...

itcprogramdev.org/itc2003proc/Papers/PDFs/0018_3c.pdf - [Similar pages](#)

Synopsys Physical Scan Synthesis Technology Backgrounder

Typically, to have **multiple** scan chains in a design, the scan cells are ...

In the Physical Compiler environment, **scan-chain** allocation within the same ...

www.synopsys.com/products/test/pss_bkgd.html - 23k - [Cached](#) - [Similar pages](#)

Applying Advanced Fault Models

These **lock-up** latches eliminate clock skews between domains while shifting through the **scan chain**. These delay the data for half a clock cycle, ...

www.evaluationengineering.com/archive/articles/0304/0304fault_models.htm - 21k - [Cached](#) - [Similar pages](#)

[PDF] Efficient Scan Chain Design for Power Minimization During Scan ...

File Format: PDF/Adobe Acrobat

scan chain with minimum test power. To tackle this NP-. hard problem efficiently, the heuristic ... **multiple** clock domains and **lockup** latches. Also, work ...

doi.ieeeecomputersociety.org/10.1109/TEST.2003.1270874 - [Similar pages](#)

